

Syllabus:

Architecture of 8085, Pin Diagram, Memory interfacing, Addressing modes, Instruction set.

“Introduction” the basic concepts:

The microprocessor is one of the most important components of a digital computer. It act as a brain of a computer system. Computers are of two types: analog computers and digital computers. A digital computer makes processing of digital signals or numbers while analog computer processes analog signals (Continuous quantity) A digital computer is a programmable machine. Its main component are: CPU (Central Processing Unit), memory, input device and output device as shown in fig1.1

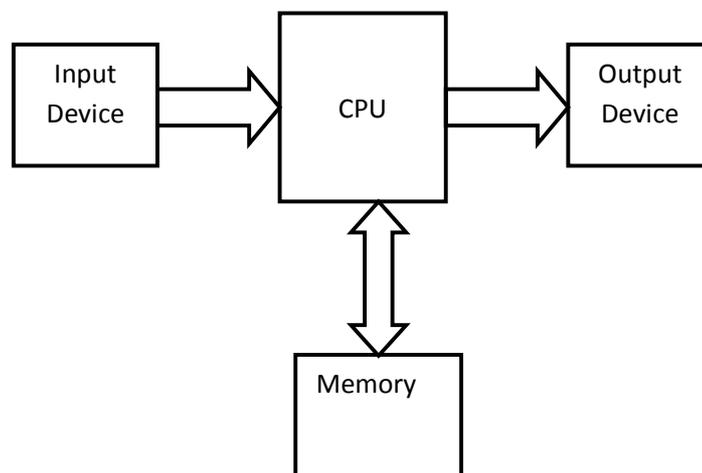


Fig. 1.1 Schematic diagram of a digital computer

The CPU executes instructions given by the programmer. The input device is used to feed programs and data to the computer. The memory is storage device. It stores programs, data and result. The output device displays or prints programs, data and/or results according to the instruction given to the computer.

“ The central Processing Unit (CPU) built on single IC is called microprocessor.”

A digital computer in which one microprocessor has been provided to act as CPU, is called **microcomputer**.

“ A microprocessor is a multipurpose, programmable, clock driven, register-based electronic device that reads binary instructions from storage device called memory, accepts binary data as input and processes data according to those instructions, and provides results as output.”

Fundamentals Of Microprocessor And Microcontroller

Unit-1

The physical component digital computer system or programmable machine are called *hardware*. A set of instructions written for microprocessor to perform a task is called a *program*, and group of programs is called *software*.

The microprocessor operates in binary digits, 0 and 1, also known as bits. Each microprocessor recognizes and processes a group of bits called the word, and microprocessors are classified according to their word length.

• Word Length of a Microprocessor:

The word length of microcomputer or microprocessor is given as “n-bit” where, n= 4, 8, 16, 32 or 64. An 8-bit microprocessor can process 8-bit data at a time. Its ALU (Arithmetic Logic Unit) is of 8 bit, its general purpose registers which holds data for processing, are 8-bit. Similarly, a 16 bit processor handles 16 bit data at a time and its ALU, general purpose registers, are of 16 bits. A processor of longer word length is more powerful and can process data at faster speed.

• History of microprocessor:

The first microprocessor INTEL 4004, a 4-bit PMOS microprocessor was introduced in the year 1971 by Intel Corporation, U.S.A. after this a 4-bit microprocessor Intel404, an enhanced version of Intel 4004 was developed. Many other companies also developed 4-bit microprocessor.

In 1972, Intel introduced the first 8-bit microprocessor, Intel 8008 which also uses PMOS technology. The microprocessor using PMOS technology were slow and not compatible with TTL logic. In 1976 Intel developed an improved version of 8-bit NMOS microprocessor, Intel 8085 which uses only one +5V.

Microprocessor	Year of introduction	Word length (bit)	Memory addressing capacity	Pins	Clock	Remarks
4004	1971	4	1 KB	16	750 KHz	First microprocessor
8085	1976	8	64 KB	40	3-6 MHz	Popular 8-bit microprocessor
8086	1978	16	1 MB	40	5-10 MHz	Popular 8-bit microprocessor
8088	1980	8/16	1 MB	40	5-8 MHz	Widely used in PC/XT
80286	1982	16	16 MB real, 4 GB virtual	68	6-12.5 MHz	Widely used in PC/AT
Pentium	1993	32	4 GB real, 32-bit address & 64-bit data bus	237 PGA	60-200 MHz	Contains 2 ALUs
Pentium Pro	1995	32	64 GB real, 36-bit address bus	387 PGA	150-200 MHz	It is data flow processor
Itanium	2001	64	64 address lines	423 PGA	733 MHz-1.5 GHz	64-bit (Explicitly Parallel Instruction Computing) Processor

Architecture of Intel 8085 Microprocessor

- **Features of 8085**
 - ✓ Intel 8085 is an 8-bit, NMOS microprocessor.
 - ✓ It is a 40 pin I.C. package fabricated on a single LSI chip.
 - ✓ The Intel 8085 uses a single +5V_{d.c.} supply for its operation
 - ✓ Its clock speed is about 3 MHz.
 - ✓ The clock cycle is of 320 ns.
 - ✓ It has 80 basic instructions and 256 opcodes.
 - ✓ Fig. 1.2 shows the functional block diagram of Intel 8085. It consists of three main sections:
 - [1] Arithmetic and Logic Unit (ALU)
 - [2] Timing & Control Unit
 - [3] Set of registers.

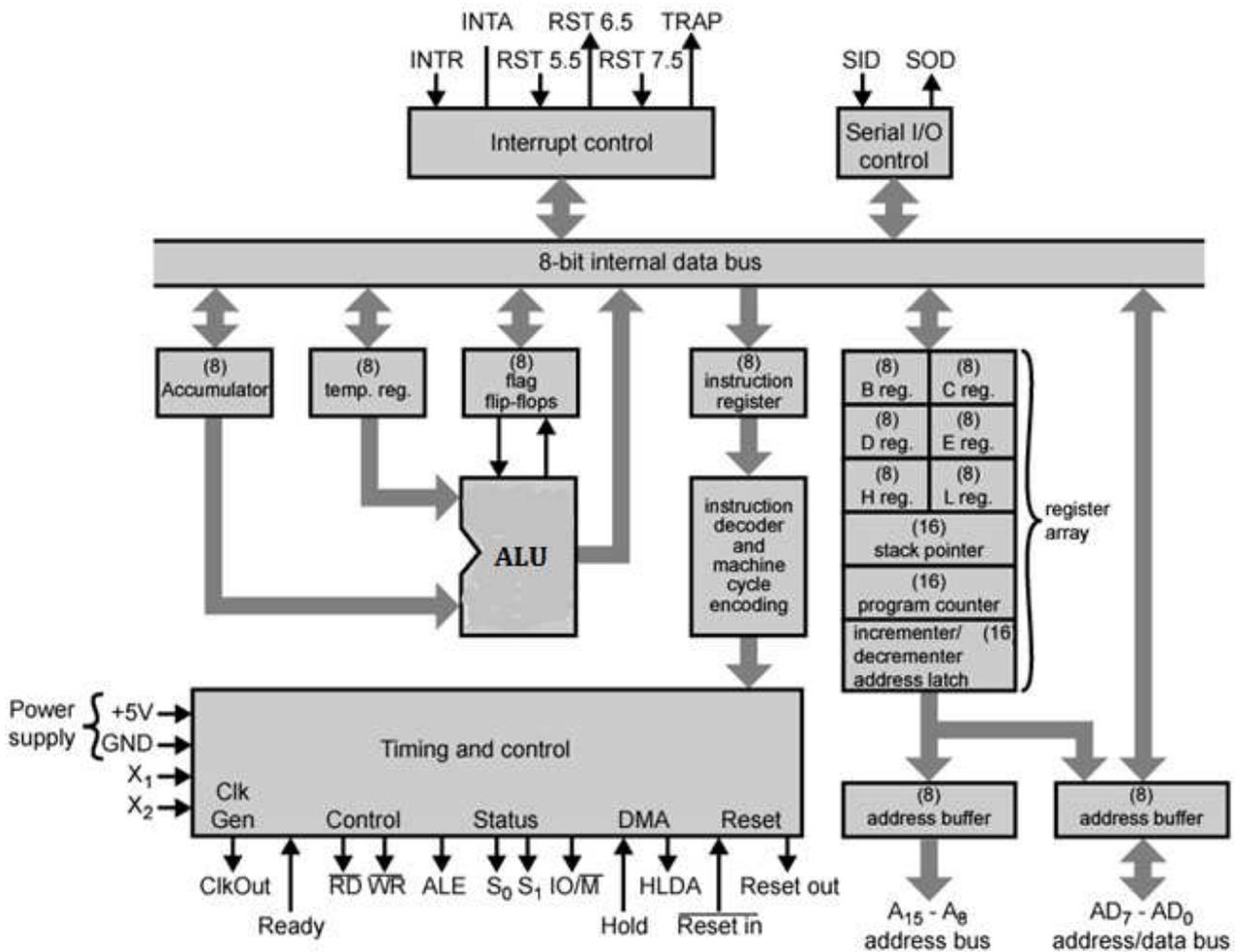


Fig. 1.2 Architecture or Functional Block Diagram of Intel 8085

1. ALU (Arithmetic & Logic Unit):

- ✓ As the name suggest, ALU i.e arithmetic & logic unit performs the following arithmetic & logical opeartions:
 - i. Addition
 - ii. Subtraction
 - iii. Logical AND
 - iv. Logical OR
 - v. Logical EXCLUSIVE OR
 - vi. Complement (logical NOT)
 - vii. Increment (add 1)
 - viii. Decrement (Subtract 1)
 - ix. Left shift, Rotate left, Rorate Right
 - x. Cler, etc.

2. Timing & Control Unit:

- ✓ It generates timing & control signals which are necessary for the execution of instructions.
- ✓ It controls data flow between CPU and peripherals including memory.
- ✓ It provides status, control and timing signals which are required for the operation of memory and I/O devices.
- ✓ It controls entire operations of the microprocessor and peripherals connected to it.
- ✓ Thus it is seen that the control unit of the CPU acts as the brain of the computer system.

3. Set of Registers:

- ✓ Fig 1.2 shows the various registers of Intel 8085 which are used by the microprocessor for temporary storage and manipulation of data and intrsuctions.
- ✓ Intel 8085 microprocessor has the following registers:
 - i. One 8-bit Accumulator (ACC) i.e register A
 - ii. Six 8-bit general purpose registers. These are B, C, D, E, H & L
 - iii. One 16-bit stack pointer, SP
 - iv. One 16-bit program Counter, PC
 - v. Intruction register
 - vi. Temporary register
- ✓ In addition to the above mentioned regiter the 8085 microprocessor contains a set of five flipflops which serve as flag (or status flags). A flag is a flipflop which indicates some condition which arises after execution of an arithmetic or logical instruction.

3.1 Accumulator:

- ✓ The accumulator (register A) is an 8-bit register associated with ALU.
- ✓ It is used to hold one of the operands of an arithmetic or logical operation.
- ✓ It serves as one input to the ALU. The other operand for an arithmetic or logical opeartion may be stored either in the memroy or in one of the general purpose registers.
- ✓ Final result of an arithmetic or logical operation is placed in the accumulator.

(note: The above description are true for general cases, not for some typical or exceptional cases. For example, there are some logical instructions which need only one operand. It is held in the accumulator. The result is placed in the accumulator. Such instruction do not require any other register or memory location because there is no other operand. There is one typical instruction DAD rp, for 16-bit addition for which one of the 16-bit operands is kept in H-L pair and the other in the B-C or D-E pair. The result is placed in the H-L pair.)

3.2 General Purpose Registers

- ✓ The 8085 microprocessor contains six 8-bit general purpose registers. They are B, C, D, E, H and L.
- ✓ To hold 16-bit data a combination of two 8-bit registers can be employed which known as register pairs.
- ✓ The valid register pairs in 8051 are B-C, D-E and H-L. the programmer can not form the register pair by selecting any two registers of his choice.
- ✓ The H-L pair is used to act as memory pointer and for this purpose it holds the 16-bit address of a memory location.
- ✓ The general purpose registers and the accumulator are accessible to programmer. He can store data in these registers during writing his program.

3.3 Program Counter (PC):

- ✓ It is a 16-bit special purpose register used to hold the memory address of the next instruction which is to be executed.
- ✓ It keeps the track of memory addresses of the instructions in the program while they are being executed.
- ✓ The microprocessor increments the content of the program counter during the execution of an instruction so that it points to the address of the next instruction in the program at the end of the execution of an instruction.

3.4 Stack Pointer (SP):

- ✓ It is a 16-bit special purpose register.
- ✓ "Stack is a sequence of memory location set aside by the programmer to store/retrieve the content of accumulator, flags, program counter and general purpose registers during the execution of a program.
- ✓ Any portion of the memory can be used as stack. Since the stack works on LIFO (last in first out) principle, its operation is faster compared normal store/ retrieve of memory locations.
- ✓ "The SP holds the address of the top element of data stored in the stack.
- ✓ "The stack is defined and stack pointer is initialized by the programmer at the beginning of a program which needs stack operation. Stack is also used by the microprocessor. For example, it stores the contents of program counter when it jumps to a subroutine using CALL instruction.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

3.5 Instruction Register:

- ✓ The instruction register holds the opcode (operation code or instruction code) of the instruction which is being decoded and executed.

3.6 Temporary Register:

- ✓ It is an 8-bit register associated with ALU. It holds data during an arithmetic/logical operation.
- ✓ It is used by microprocessor.
- ✓ It is not accessible to programmer.

3.7 Flags (Program Status Word i.e PSW):

- ✓ The Intel 8085 microprocessor contains five flipflops to serve as status flags.
- ✓ The flip-flops are set or reset according to the conditions which arises during an arithmetic or logical operation.
- ✓ The five status flags of Intel 8085 are:
 - Carry flag (CS)
 - Parity Flag (P)
 - Auxiliary Carry Flag (AC)
 - Zero Flag (Z)
 - Sign Flag (S)
- ✓ In fig 1.3, five bits indicates the five status flags and three bits are undefined. “ The combination of these 8-bits is called **Program Status Word (PSW)**”. PSW and the accumulator are treated as a 16-bit unit for stack operation.

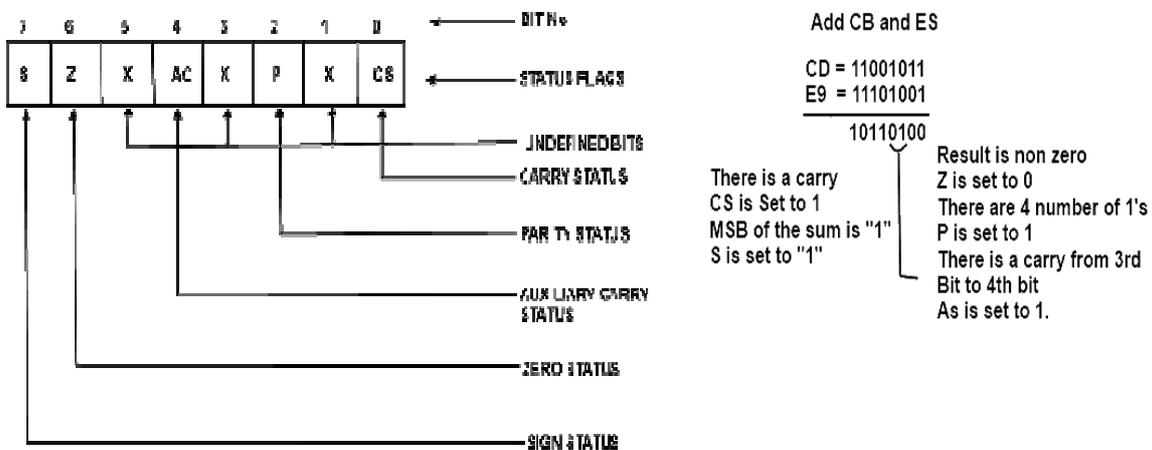


Fig 1.3 Program Status Word

• Carry Flag (CS):

- ✓ After execution of an arithmetic instruction if carry is produced, the carry flag CS is set to 1. Otherwise it is 0.
- ✓ The carry flag is set or reset in case of addition as well as subtraction.
- ✓ After the addition of two 8-bit numbers, if the sum is larger than 8-bits, a carry is produced; and the carry flag is set to 1.
- ✓ In case of subtraction, if borrow occurs, the carry flag is set to 1.
- ✓ The carry flag holds carry out of the most significant bit resulting from the execution of an arithmetic operation.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

- **Prity Flag (P):**
 - ✓ The parity flag P is set to 1, if the result of an arithmetic or logical opeartion contains even number of 1s.
 - ✓ It is reset i.e it is 0, if the result contains odd number of 1s.
- **Auxiliary Carry Flag (AC):**
 - ✓ The auxiliary carry flag AC hold carry out of the bit number 3 to the bit number 4 resulting from the execution of an arithmetic operation.
 - ✓ The counting of bits starts from 0, and hence Bit No.3 is actually the fourth bit from the least significant bit.
- **Zero Flag (Z):**
 - ✓ The zero status flag Z is set to 1, if the result of an arithmetic or logical operation is Zero otherwise it is set to 0.
- **Sign Flag (S):**
 - ✓ The sign flag S is set to 1, if the result of an arithmetic or logical operation is negative. If the result is positive, the sign flag is set to 0.
 - ✓ The sign flag has significance only when signed arithmetic operation is performed. To represen a signed numbet the most significant bit is reserved by the programmer to represent the sign of a number.
 - ✓ In other words the MSB is used as asign bit.
 - ✓ If the number is negative, the sign bit is 1. For positive, sign bit is 0.
 - ✓ In case of 8-bit sign operation, the remaining 7 bits are used to represent the magnitude of a number.

3.8 Data and Address bus:

- ✓ The Intel 8085 is an 8-bit microprocessor. Its data bus is 8-bit wide and hence, 8bit of data can be tyransmitted in parallel from or to the microprocessor.
- ✓ The Intel 8085 requires a 16 bit wide address bus as the memory addresses are of 16 bits.
- ✓ The 8 most significant bits of the address are transmitted by the address bus, a-bus (pins A₈ to A₁₅).
- ✓ The least significant bits of address are transmitted by address/ data bus, AD-bus (pins AD₀ to AD₇).
- ✓ The address/ data bus transmits data and address at different moments. At a perticular moment it transmits either data or address. Thus AD-bus operates in time shared mode.
- ✓ This technique is known as multiplexing.first all 16-bit memory address is transmitted by the microprocessor; the 8 MSBs of the address on A-bus and the 8 LSBs of the address on AD-bus. Thus effective width of address bus becomes 16 bit wide.

Pin Diagram of 8085

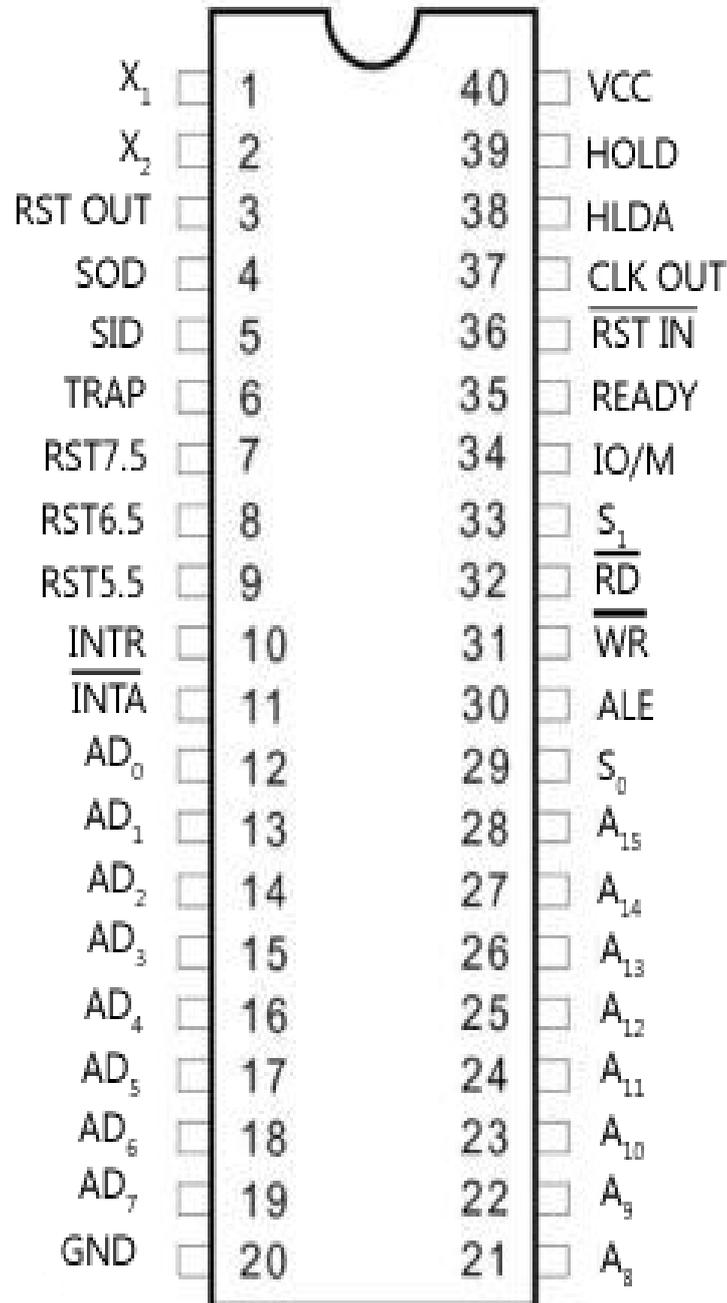


Fig 1.4 Pin Diagram of 8085

Fig. 1.4 Shows the schematic diagram of 8085.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

The description of various pins is as follows.

A₈ – A₁₅ :

- ✓ These are the output lines
- ✓ These are the parallel address lines called as Address bus and are used for the most significant bits of the memory address or 8 bits of I/O address.

AD₀ – AD₇ :

- ✓ Input / Output lines
- ✓ These are time multiplexed address/data bus *i.e.* they serve dual purpose.
- ✓ They are used for the least significant 8 bits of memory address or I/O address during the first clock cycle of a machine cycle.
- ✓ Again they are used for data during second and third clock cycles.

ALE:

- ✓ It is an output pin.
- ✓ It is an address latch enable signal.
- ✓ It goes high during first clock cycle of a machine cycle and enables the lower 8 bits of the address to be latched either in to the memory or external latch.

IO/ \overline{M} :

- ✓ It is an output status signal which distinguishes whether the address is for memory or I/O.
- ✓ When it goes high the address on the address bus is for an I/O device.
- ✓ When it goes low the address on the address bus is for a memory location.

S₀, S₁ :

- ✓ These are the output status signals sent by the microprocessor to distinguish the various types of operations as given below.

Status codes for 8085

S ₁	S ₀	Operation
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

\overline{RD} :

- ✓ It is an output control signal.
- ✓ It controls the READ operation.
- ✓ When it goes low selected memory or I/O device is read.

\overline{WR} :

- ✓ It is an output control signal.
- ✓ It controls the WRITE operation.
- ✓ When it goes low data on the data bus is written into the selected memory or I/O location.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

READY: (input)

- ✓ It is used by the microprocessor to sense whether a peripheral is ready to transfer data or not.
- ✓ A slow peripheral may be connected to the microprocessor through READY line.
- ✓ If READY is high peripheral is ready.
- ✓ If it is low microprocessor waits till it goes high.

HOLD (input):

- ✓ It indicates that another device is requesting for the use of address and data bus.
- ✓ After receiving the HOLD request microprocessor handover the controls of buses to that devices as soon as current machine cycle is completed. Internal processing may continue.
- ✓ The processor regains the control over the buses after removal of HOLD signal.
- ✓ When hold is acknowledged, address bus, data bus, \overline{RD} , \overline{WR} , and IO/\overline{M} are tri-stated.
- ✓ HOLD is sampled in T_2 Clock Cycle.

HLDA (output):

- ✓ It is signal for HOLD acknowledgement.
- ✓ It indicates that the HOLD request has been received.
- ✓ After removal of a HOLD request the HLDA goes low.
- ✓ The CPU takes over the buses half clock cycle after the HLDA goes low.

INTR (input):

- ✓ It is an interrupt request signal.
- ✓ Among interrupts it has lowest priority.
- ✓ When it goes high the program counter does not increment its content.
- ✓ The microprocessor suspends its normal sequence of instructions.
- ✓ After completing the instruction at hand it attends the interrupting device.
- ✓ The INTR line is sampled in the last state of the last machine cycle of an instruction.
- ✓ The INTR is enabled or disabled by software.
- ✓ An interrupt is used by I/O device to transfer data to microprocessor without wasting time.
- ✓ If CPU is in HOLD state or interrupt enable flip-flop is reset, an interrupt request is not honoured.

\overline{INTA} : (output)

- ✓ It is an interrupt acknowledgement sent by the microprocessor after INTR is received.

RST 5.5, 6.5 and TRAP: (inputs)

- ✓ These are the interrupts.
- ✓ When an interrupt is recognized the next instruction is executed from a fixed location in the memory as given below:

Fundamentals Of Microprocessor And Microcontroller

Unit-1

Line	Location from which next instruction is picked up (vectored location)
TRAP	0024
RST 5.5	002C
RST 6.5	0034
RST 7.5	003C

- ✓ RST 7.5, RST6.5 and RST 5.5 are the restart interrupts. They cause an internal restart to be automatically inserted, Each them has programmable mask.
- ✓ The TRAP has highest priority among the interrupts and it is nonmaskable interrupt.
- ✓ The order of priority of interrupts is as follows:
 - TRAP (Highest Priority)
 - RST7.5
 - RST6.5
 - RST5.5
 - INTR (Lowest Priority)

RESET IN: (input)

- ✓ It resets the program counter to 0.
- ✓ It also resets interrupt enable and HLDA flip-flops.
- ✓ It does not affect any other flag or register except the instruction register.
- ✓ The CPU is held in reset condition as long as RESET is applied.

RESET OUT: (output)

- ✓ It indicates that the CPU is being reset.

X₁, X₂: (input)

- ✓ These are terminals connected to an external crystal oscillator which drives an internal circuitry of the microprocessor to produce a suitable clock for the operation of microprocessor.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

CLK: (output)

- ✓ It is a clock output for user, which can be used for other digital ICs. Its frequency is same at which microprocessor operates.

SID : (input)

- ✓ It is a data line for serial input.
- ✓ The data on this line is loaded into the 7th nit of the accumulator when RIM instruction is executed.

SOD: (output)

- ✓ It is a data line for serial output. The 7th bit of the accumulator is output on SOD line whwn SIM instruction is executed.

V_{cc}:

- ✓ +5 volts supply.

V_{ss}:

- ✓ Ground reference.

“Memory Interfacing Introduction” Basic Concept before interfacing

Memory Structure and Its Requirements:

- ✓ Read/Write memory is a group of registers to store binary information. Fig 1.5 (a) shows a typical R/W memory chip; it has “ $2^n = M$ ” registers (where n= no. of address lines) and each can store N no. of bits.
- ✓ It has N no. of bidirectional (or separate input-output) data lines.
- ✓ It also has one Chip select (\overline{CS}), and two control lines Read (\overline{RD}) to enable the output buffer and Write (\overline{WR}) to enable the input buffer.
- ✓ Fig. 1.5 (b) shows the logic diagram of typical EPROM (Erasable Programmable Read Only Memory with “ $2^n = M$ ” registers (where n= no. of address lines).
- ✓ It has “n” no. of address lines, one Chip select (\overline{CS}) and one Read (\overline{RD}).
- ✓ This memory chip must be programmed before it can be used as Read-Only memory.

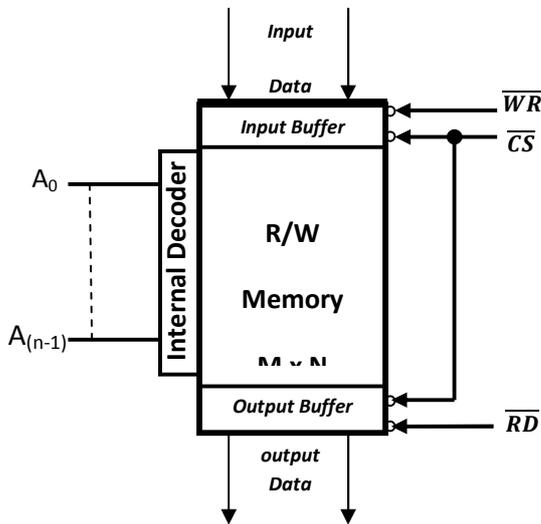


Fig 1.5 (a) Typical R/W memory

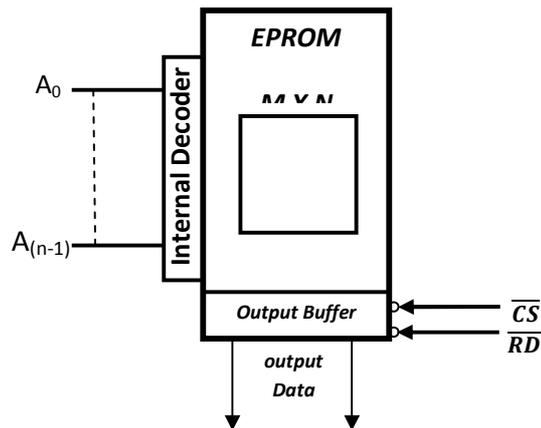


Fig 1.5 (b) Typical EPROM

The 8085 microprocessor uses a 16-bit wide address bus for addressing memories and I/O devices. Using 16-bit wide address bus it can access $2^{16} = 64K$ bytes of memory and I/O devices. The 64K addresses are to be assigned to memories and I/O devices for their addressing. There are two schemes for the allocation of addresses to memories and input / output devices:

1. Memory mapped I/O scheme.
2. I/O mapped I/O scheme.

Memory mapped I/O scheme:

- ✓ In memory mapped I/O scheme there is only one address space.
- ✓ Address space is defined as the set of all possible addresses that microprocessor can generate.
- ✓ Some addresses are assigned to memories and some addresses to I/O devices.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

- ✓ An I/O device is also treated as memory location and one address is assign to it.
- ✓ Suppose that memory locations are assigned the addresses 2000 H to 24FF H then each one address is assign to each memory location. The addresses for I/O devices are different from the addresses which have been assigned to memories.
- ✓ The addresses which have not been assigned to memories can be assigned to each I/O device.
- ✓ In this scheme all the data transfer instructions of the microprocessor can be valid for data transfer from the memory location or I/O device whose address is in H-L pair.

I/O mapped I/O scheme:

- ✓ In this scheme the addresses assigned to memory location can also be assigned to I/O devices.
- ✓ Since the same address may be assigned to memory location or an I/O device, the microprocessor must issue a signal to distinguish whether the address on the address bus is for a memory location or an I/O device.
- ✓ The 8085 issues an $\overline{IO/\overline{M}}$ signal for this pupose.
- ✓ Two extra instructions IN and OUT are used to address I/O devices.

Demultiplexing the Bus AD – AD₀ :

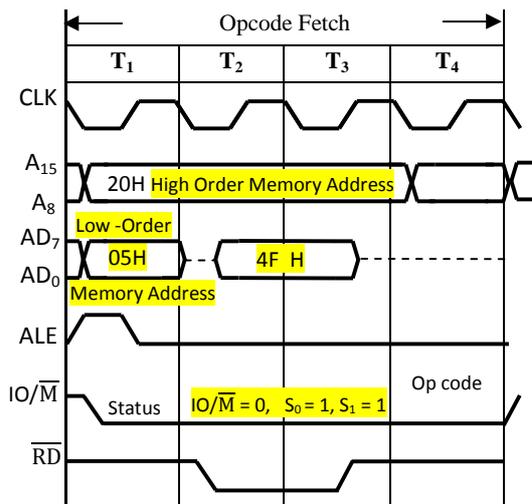


Fig. 1.6 Timing Diagram : Transfer of Byte from Memory to Microprocessor

- ✓ Fig 1.6 shows the timing diagram of how a data byte is transferred from memory to the microprocessor from which the need for demultiplexing the bus AD₀-AD₇ becomes easier to understand.
- ✓ This figure shows that the address on the high order bus (20H) remains on the bus for three clock periods.
- ✓ However, the low order address (05H) is lost after the first clock period.
- ✓ This address needs to be latched and used for identifying the memory address.
- ✓ If the bus AD₇-AD₀ is used to identify the memory location (2005H), the address will change to 204FH after the first clock period.
- ✓ Fig. 1.6 shows a schematic that uses a latch and the ALE signal to demultiplex the bus. The bus AD₇-AD₀ is connected as input to latch 74LS373.

Fundamentals Of Microprocessor And Microcontroller

Unit-1

- ✓ The ALE signal is connected to Enable (G) pin of the Latch, and the Output control (\overline{OC}) signal of the latch is grounded.
- ✓ Fig 1.6 shows that the ALE goes high during T_1 . When the ALE is high, the latch is transparent; that means output changes according to the input data.
- ✓ During T_1 output of the latch is 05H.
- ✓ When ALE goes low, the data byte 05H is latched until the next ALE, and the output of the latch represents the low-order address bus A_7-A_0 after the latching operation.

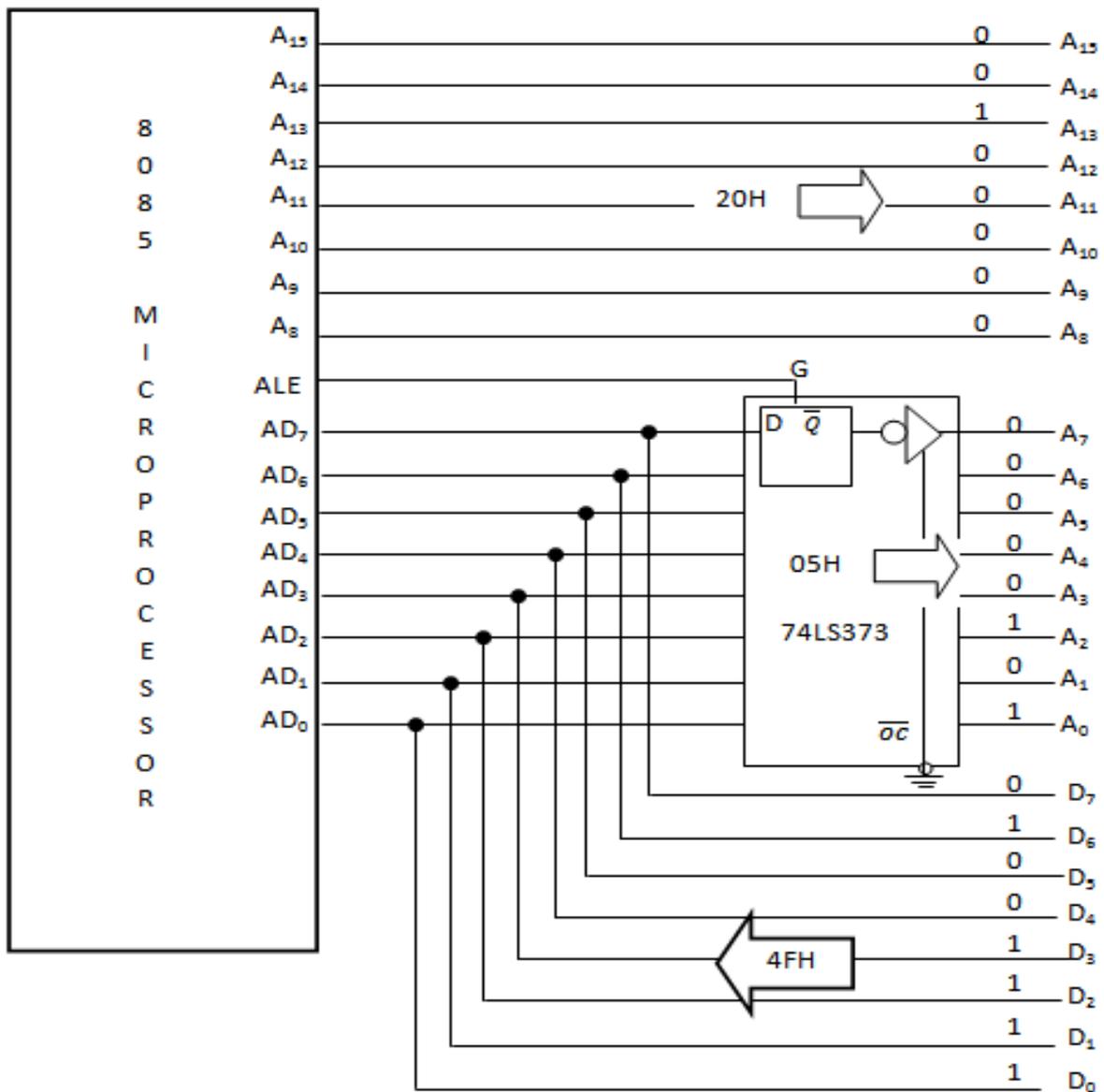


Fig. 1.7 Schematic of Latching Low-Order Address Bus

Fundamentals Of Microprocessor And Microcontroller

Unit-1

Generating Control Signals:

- ✓ Fig 1.6 shows the \overline{RD} (Read) as a control signal. Because this signal is used both for reading memory and for reading an input device, it is necessary to generate two different Read signals: one for memory and another for input. Similarly, two separate Write signals must be generated.
- ✓ Fig 1.8 shows that four different control signals are generated by combining the signals \overline{RD} , \overline{WR} and IO/\overline{M} . The signal IO/\overline{M} goes low for the memory operation.
- ✓ This signal is ANDed with \overline{RD} and \overline{WR} signals by using the 74LS32 quadruple two-input OR gates, as shown in Fig 1.7.
- ✓ When both the input goes low, the outputs of the gates go low and generate \overline{MEMR} (memory Read) and \overline{MEMW} (memory Write) control Signals.
- ✓ When IO/\overline{M} goes high, it indicates the peripheral I/O operation. Fig. 1.8 shows that this signal is complemented and ANDed with \overline{RD} and \overline{WR} signals to generate \overline{IOR} (I/O Read) and \overline{IOW} (I/O Write) control Signals.
- ✓

IO/\overline{M}	\overline{RD}	\overline{WR}	Control Signal
0	0	1	Memory read
0	1	0	Memory write
1	0	1	I/O read
1	1	0	I/O write

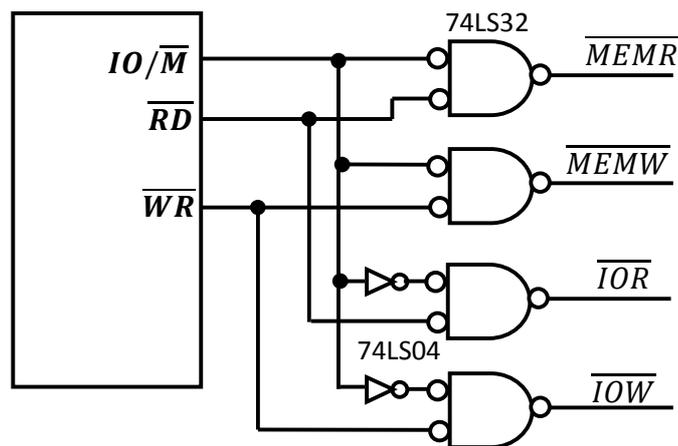


Fig 1.8 Schematic to Generate Read/Write Control Signals for Memory and I/O
 Note: the control signals can also be generated using decoder IC for ex. 74LS138

Fundamentals Of Microprocessor And Microcontroller

Unit-1

Address Decoding:

- ✓ The address of a memory location is sent out by the microprocessor. The corresponding memory chip or I/O device is selected by a decoding circuit.
- ✓ The decoding task can be performed by a decoder, a comparator, a bipolar PROM or PLA (Programmed logic array).
- ✓ For memory interfacing we can use Decoder IC 74LS138 which has G1, G2A and G2B enable signals.
- ✓ To enable 74LS138, G1 should be high, and G2A and G2B should be low. Also, 74LS138 has three select lines A, B & C. By applying proper logic to select lines any one of the output can be selected.
- ✓ Where, 74LS138 has Y₀, Y₁,Y₇ output lines. An output line goes low when it is selected. Other output lines remain high. Thus as shown in Table 1.1 (Truth table for 74LS138), when G1 is low or G2A is high or G2B is high, all output lines become high.
- ✓ Thus 74LS138 acts as decoder only when G1 is high, and G2A and G2B are low.

Fig 1.1 Truth table for 74LS138

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2A	G2B	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	H	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

- ✓ As shown in the fig. 1.8 the memory location for the memory whose chip select is attached to Y₁ output of the decoder 74LS138 will lie in the range of 1000 to 1FFFH

(this address range is for given connection by various combination of connection we can vary the address range for the same memory chip as per requirement. Also refer the following table 1.1 and table 1.2 for address calculated in the fig 1.8)

	To Decoder				To memory chip											
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Starting Address	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
End Address	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 1.2 Address range calculation

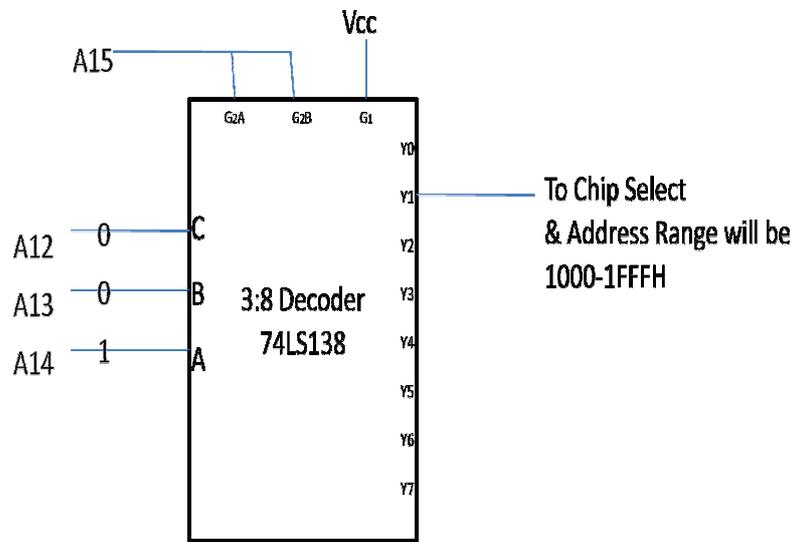
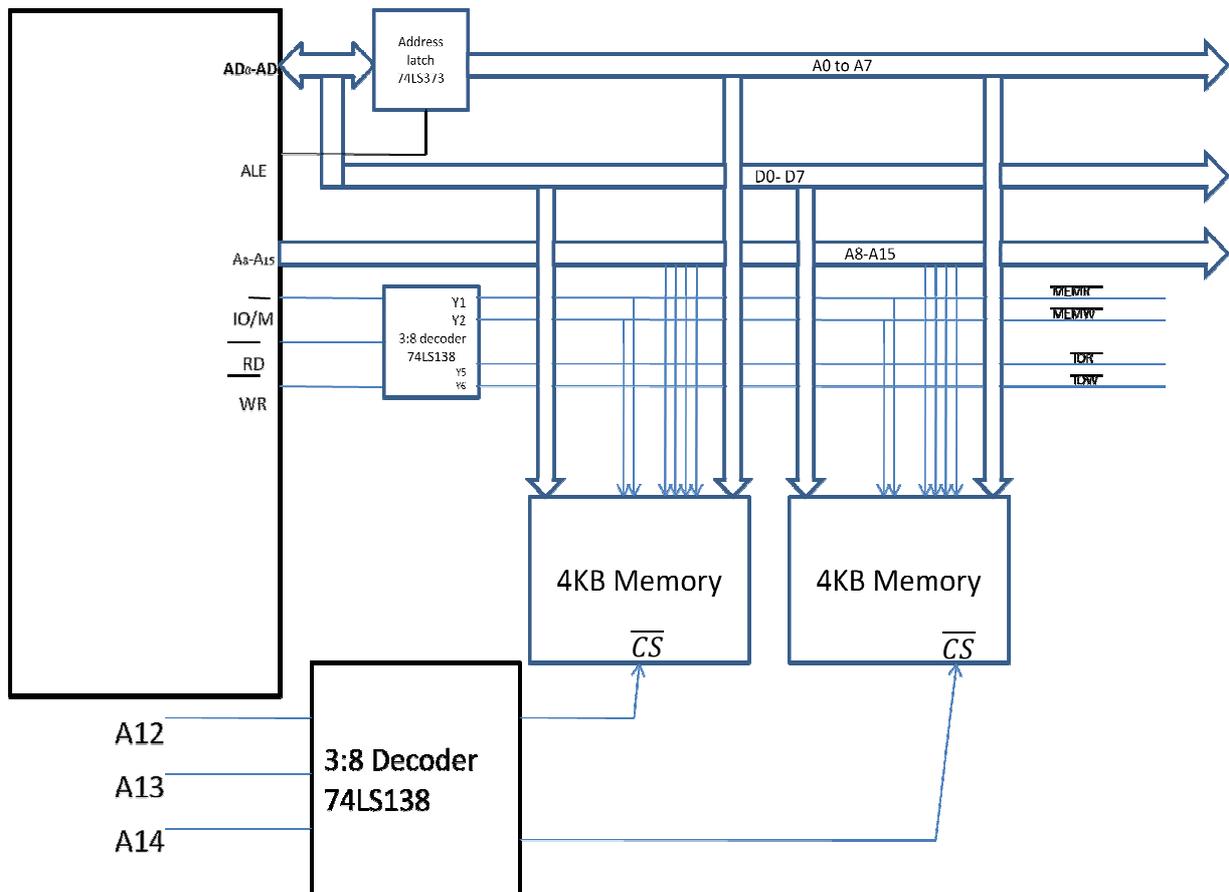


Fig. 1.8 Address Decoding Using 74LS138

Following fig shows the simple interfacing of 8K memory with 8085



“Addressing Modes ”

Introduction:

Each instruction requires certain data on which it has to operate. The various techniques to specify data for instruction are called Addressing Modes.

The 8085 has following addressing modes:

1. **Direct Addressing**
2. **Register Addressing**
3. **Register indirect Addressing**
4. **Immediate Addressing**
5. **Implicit Addressing**

1. Direct Addressing Mode:

- ✓ In this mode of addressing the *address of the operand (data)* is given in the instruction itself.

Examples are:

- [1] **STA 2400H** Store the content of the accumulator in the memory location 2400H.
32,00,24 The above instruction in code form.

In this instruction 2400H is the memory location where data is to be stored. It is given in the instruction itself. The 2nd and 3rd byte of the instruction specify the address of the memory location. Here, it is understood that the source of the data is accumulator.

- [2] **IN 02H** Read data from port C.
DB,02 Instruction in code form.

In this instruction 02H is the address of Port C of an I/O port from where the data is to be read. Here, it is implied that the destination is the accumulator. The 2nd byte of the instruction specifies the address of the port.

2. Register Addressing Mode:

- ✓ In register addressing mode the operand is in one of the general purpose registers. The opcode specifies the address of the register(s) in addition to the operation to be performed.

Examples are:

- [1] **MOV A, B** Move the content of register B to register A.
78 The above instruction in code form.

The opcode for MOV A, B is 78H. Besides the operation to be performed the opcode also specifies source and destination registers. The opcode 78H can be written in binary form as 01111000. The first two bits, i.e 01 are for MOV operation, the next three bits 111 are the binary code for register A, and the last three bits 000 are the binary code for register B.

- [2] **IN 02H** Read data from port C.
DB,02 Instruction in code form.

In this instruction 02H is the address of Port C of an I/O port from where the data is to be read. Here, it is implied that the destination is the accumulator. The 2nd byte of the instruction specifies the address of the port.

Fundamentals Of Microprocessor And Microcontroller

Unit-1
